EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Larry S. Nixon, Reg. No. 25,640 on 05/16/2011.

3. Pursuant to MPEP 606.01 the title has been changed to read:

-- A COMMON PROGRAM FOR SWITCHING BETWEEN OPERATION SYSTEMS IS EXECUTED IN CONTEXT OF THE HIGH PRIORITY OPERATING SYSTEM WHEN INVOKED BY THE HIGH PRIORITY OS --

4. Please amend the specification as following:

a. page 1, line 21, change "program" to --programs--;

b. page 1, line 24, delete "the"

c. page 5, line 5, change "retrieve" to --retrieved--;

d. page 5, line 11, change "the Intel" to --Intel--

5. The following claim had been amended:

This listing of claim will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of enabling multiple different operating systems to run concurrently on the same computer, comprising:

selecting a first operating system to have a relatively high priority, said first operating system possibly being a real time operating system;

selecting at least one second operating system to have a relatively lower priority;

providing a common program arranged to switch between said operating systems under predetermined conditions, the common program being arranged to save, and to restore from a saved version, the processor state required to switch between the operating systems; ~~and~~

providing modifications to said first and second operating systems to allow them to be controlled by said common program,

wherein the first and second operating systems are associated with first and second memory contexts, respectively, and the common program is associated with a third memory context,

switching a current memory context to the first memory context when switching to or from the first operating system; and

switching the current memory context to the third memory context when switching from the second operating system;

wherein, when the common program is invoked by the first operating system, execution of the common program is started in the first memory context, and

wherein, when the common program is invoked by the second operating system, ~~the current memory context is the third memory context, thereby~~ using the third memory context as an intermediate address space.

2. (Previously Presented) The method of claim 1, comprising switching ~~a~~ the current memory context to the first, second or third memory context when switching between said operating systems.

3-4. (Cancelled)

5. (Previously Presented) The method of claim 1, further comprising preempting the first operating system by the common program, and starting execution of the common program in the first memory context.

6-7. (Cancelled)

8. (Previously Presented) The method of claim 1, further comprising preempting the second operating system by the common program, wherein the current memory context is the third memory context.

9. (Previously Presented) The method of claim 8, wherein the second operating system invokes the common program by a trap call.

10. (Previously Presented) The method of claim 1, in which the first operating system is a real time operating system.

11. (Previously Presented) The method of claim 1, in which the second operating system is a non-real time, general-purpose operating system.

12. (Previously Presented) The method of claim 1, in which the second operating system is Linux, or a version or variant thereof.

13. (Cancelled)

14. (Previously Presented) The method of claim 1, in which processor exceptions for the second operating system are handled in virtual fashion by the common program.

15. (Previously Presented) The method of claim 1, in which the common program is arranged to intercept some processor exceptions, and to call exception handling routines of the first operating system to service them.

16. (Previously Presented) The method of claim 1, in which the processor exceptions for the second operating system are notified as virtual exceptions.

17. (Original) The method of claim 16, in which the common program is arranged to call an exception handling routine of the second operating system corresponding to a said virtual exception which is pending.

18. (Previously Presented) The method of claim 1, further comprising providing each of said operating systems with separate memory spaces in which each can exclusively operate.

19. (Previously Presented) The method of claim 1, further comprising providing each of said operating systems with first input and/or output devices of said computer to which each has exclusive access.

20. (Previously Presented) The method of claim 1, in which each operating system accesses said first input and/or output devices using substantially modified native routines.

21. (Previously Presented) The method of claim 1, further comprising providing each of said operating systems with access to second input and/or output devices of said computer to which each has shared access.

22. (Previously Presented) The method of claim 21, in which all operating systems access said second input and/or output devices using the routines of the first operating system.

23. (Previously Presented) The method of claim 1, further comprising providing a restart routine for restarting a said second operating systems without interrupting operation of said first, or said common program.

24. (Previously Presented) The method of claim 21, in which said second device comprises a co-processor, and in which, on switching between said first operating system and said second (or vice versa), the state of said co-processor is not changed, whereby if said operating systems switch back without intervening access to said coprocessor, its operation can complete uninterrupted.

25. (Original) The method of claim 1, in which one or more original address tables are provided by the computer for use by an operating system, and in which the common program accesses said original address tables, and provides a plurality of replicated tables having the same structure as said original tables, elsewhere in memory, one per table per operating system, each for use by a respective operating system, and in which said operating systems are modified so as to replace instructions which write said original address tables with routine calls which access said replicated tables.

26. (Previously Presented) The method of claim 1, further comprising combining said operating systems and common program into a single code product.

27. (Previously Presented) The method of claim 1, further comprising embedding said operating systems and common program onto persistent memory on a computer product.

28. (Previously Presented) The method of claim 1, in which each said operating system is provided with an idle routine, in which it passes control to the common program.

29. (Previously Presented) The method of claim 28, in which said idle routine substitutes for a processor halt instruction.

30. (Previously Presented) A development kit computer program product stored in a memory and comprising code that, when executed by a processor, performs the steps of claim 1.

31. (Cancelled)

32. (Previously Presented) An embedded computer system comprising a CPU, memory devices and input/output devices, having stored on persistent memory therein programs embedded according to claim 30.

33. (Currently Amended) A computer system comprising a CPU, memory devices and input/output devices, having executing thereon computer code comprising:

a first operating system having a relatively high priority, said first operating system possibly being a real time operating system;

a second operating system having a relatively lower priority; and

a common program arranged to run said operating systems concurrently by switching between said operating systems under predetermined conditions, the common program being arranged to save, and to restore from a saved version, the processor state required to switch between the operating systems;

wherein the first and second operating systems are associated with first and second memory contexts, respectively, and the common program is associated with a third memory context,

wherein when switching to or from the first operating system, a current memory context is switched to the first memory context;

wherein when switching from the second operating system, the current memory context is switched to the third memory context;

wherein, when the common program is invoked by the first operating system, execution of the common program is started in the first memory context, and

wherein, when the common program is invoked by the second operating system, ~~the current memory context is the third memory context, thereby~~ using the third memory context as an intermediate address space.

34. (Previously Presented) A computer system according to claim 33, arranged to run said first and second operating systems concurrently using the method as described above.

35. (Currently Amended) A computer system comprising a processor and a memory ~~and operable~~ to execute thereon computer code to operate first and second operating systems in first and second memory contexts, respectively, said first operating system possibly being a real time operating system and a common program ~~operable~~ configured to execute in said first or a third memory context to switch between the first and second operating systems, the common program being arranged to save, and to restore from a saved version, the processor state required to switch between the operating systems; wherein, when the common program is invoked by the first operating system, execution of the common program is started in the first memory context,

wherein when switching to or from the first operating system, a current memory context is switched to the first memory context;

wherein when switching from the second operating system, the current memory context is switched to the third memory context; and

wherein, when the common program is invoked by the second operating system, ~~the current memory context is the third memory context, thereby~~ using the third memory context as an intermediate address space.

36. (Currently Amended) The ~~system, product or~~ method of claim 1 in which the computer has a Complex Instruction Set architecture.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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